







Grid-Connected PV Systems Design and Installation

Revisions to the Grid-Connected PV Systems: Design and Installation Australian Edition Version 8.7 Publication



Following is the summary of changes to the information within Grid-Connected PV Systems Design and Installation Australian Edition Version 8.7, August 2020. Please note that the changes in this document are subject to alterations in newer editions. While all care has been taken to ensure this document is free from omission and error, no responsibility can be taken for the use of this information in the design or installation of any grid-connected PV system.

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Keywords

Addition: Adding an additional paragraph.

Replacement: To entirely replace something.

Extension: To add an additional sentence/s onto the end of a sentence or paragraph.

Amendment: To modify sections of a paragraph or sentence either by quote or by reviewing the referenced text.

Removal: To remove something altogether.

Chapter 4

1. Section 4.4 - Combining Solar Modules

Addition:

DID YOU KNOW?

Most modern PV modules use "half-cut cells", meaning each solar cell is cut in half before they are combined in series and parallel to form a module. For more information on half-cut cell PV modules, see Section 6.3 and Section 6.4.

2. Extension Material - How a Solar Cell Works

Addition after Figure 4.21:

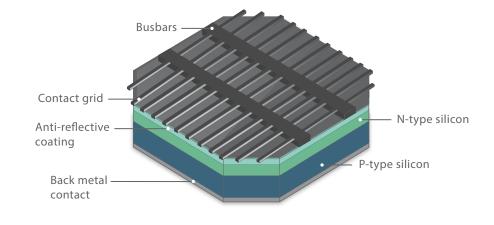


Figure 4.22: Structure of a typical commercial silicon PV cell (not to scale).

Chapter 6

3. Section 6.1.4 - Cell and Module Efficiencies

Amendment to Example:

EXAMPLE

A 1.6 kW PV array is to be designed by a system designer. The designer has a choice of two different modules. The proposed modules have different rated powers and efficiencies (shown below), but both have similar physical dimensions. What will be the difference in the power output of the array? Module one has a rated power of 320 W and an efficiency of 19.0%. Module two has a rated power of 400 W and an efficiency of 22.6%.

Array one will be composed of 5×320 W modules, with a rated power of 1.6 kW.

Array two will be composed of 4×400 W modules, with a rated power of 1.6 kW.

Therefore, the array will be rated at 1.6 kW and produce 1.6 kW at STC regardless of which modules are used. However, using the lower efficiency modules will mean that an extra module is required to reach 1.6 kW and so possibly additional cost as well as more space and mounting equipment will be required.

4. Section 6.2 - Monocrystalline Cells

Addition to Efficiency and Cost:

Many monocrystalline and polycrystalline PV modules now use Passivated Emitter and Rear Cell designed cells, or PERC cells. In PERC cells, a very thin passivation layer is introduced between the base silicon wafer and the metal contact on the rear surface, with gaps in the passivation layer allowing for small areas of direct metal contact with the wafer. This reduces the opportunity for system loss in the form of surface recombination of electrons and increases cell efficiency. The PERC structure also allows for more light absorption through rear surface reflection while simultaneously reflecting more infrared energy out of the cell. Modules using PERC technology may be more susceptible to increased degradation over their lifetime however, this is an ongoing area of research in the industry.

5. Section 6.2.2 - Polycrystalline Cells

Addition to Efficiency and Cost:

Like monocrystalline modules, polycrystalline modules can use the PERC architecture for increased efficiency.

6. Section 6.3 - Manufacturing Solar Modules

Addition to Crystalline Modules:

For half-cut cell modules, each cell is cut in half to form 120 or 144 smaller cells, which are then connected in series and parallel (Figure 6.15b). Each half-cut cell produces the same voltage as a standard cell but only half the current, thus they are arranged in two parallel strings to mimic the voltage and current ratings of a conventional module.

The conventional or half-cut cells are arranged in a grid, interconnected with metal ribbon and 'laminated' between glass at the front, an encapsulant at the back, and any backing sheet used.

7. Section 6.3 - Manufacturing Solar Modules

Replacement of Figure 6.15:

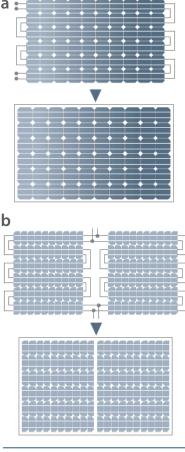


Figure 6.15: Cells in a crystalline module are connected and then encapsulated and framed.

a) a conventional module and b) a half-cut cell module.

8. Section 6.3 - Manufacturing Solar Modules

Addition:

DID YOU KNOW?

The current through each half-cut cell is lower than in a conventional cell, resulting in lower resistivity losses and higher module efficiency.

9. Section 6.4.1 - Bypass diodes

Addition:

Half-cut Cells

Like conventional modules, half-cut cell modules typically have three bypass diodes, but they are located in the middle of the module and divide the 120 or 144 half-cells into six 20 or 24 cell strings. In specific situations of localised shading a conventional module and half-cut cell module will perform similarly (Figure 6.21a). However, in most situations, for example where the bottom half of the module is shaded, the bypass diodes in a half-cut cell module will perform better than a conventional module (Figure 6.21b).

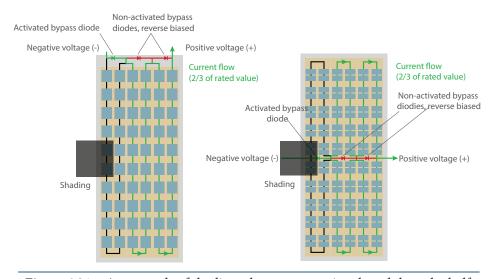


Figure 6.21a: An example of shading where a conventional module and a halfcut cell module are similarly affected.

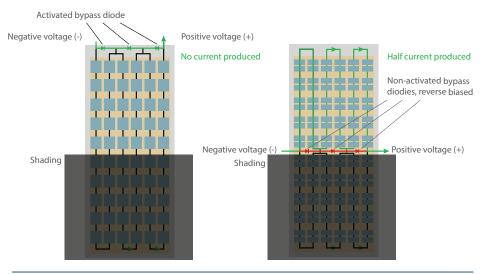


Figure 6.21b: An example of shading where a half-cut cell module outperforms a conventional module.

10. Section 6.5.4 - Hot Spots

Addition:

DID YOU KNOW?

In half-cut cell modules, the current through each cell is lower, which reduces the risk of hot spots.

Chapter 12

11. Section 12.3.1 - Using Voltage Temperature Coefficients

Amendment to Example 3:

Use the temperature coefficient for V_{oc} : This is the simplest method and will give an approximate estimate. It can be used for rough estimations, but not full design calculations.

Chapter 14

12. Section 14.1.2 - Voltage Drop and CSA

Amendment:

The maximum permissible AC voltage rise, i.e. between the inverter and the grid's point of supply, must not exceed 2% under maximum current conditions. It is recommended that the voltage rise between the inverter and the main switchboard does not exceed 1%.

13. Section 14.1.2 - Voltage Drop and CSA

Amendment to voltage drop equation:

I = Current flow (in A). For PV DC cables, the I_{sc} current (at STC) should be used.

14. Section 14.2.1 - String Cables

Amendment to Example 2:

The MPP voltage of a string at STC is 216 V, and the short circuit current is 5 A.

15. Section 14.2.2 - Sub-array Cables

Amendment to Example:

The V_{MPP} at STC of each string is 216 V and the short circuit current in the string is 5 A.

16. Section 14.2.3 - Array Cables

Amendment to Example:

The V_{MPP} at STC of each string is 216 V and the string short circuit current is 5 A.

17. Chapter 14 Quiz

Amendment to Question 1b:

According to AS/NZS 4777.1:2016, what is the maximum allowable AC voltage rise between the inverter and the point of supply?

Replacement of:

Module I_{MP}

With:

Module I_{sc}

Chapter 16

18. Section 16.2.2 - System Design and Drawings

Replacement of Figure 16.6a:

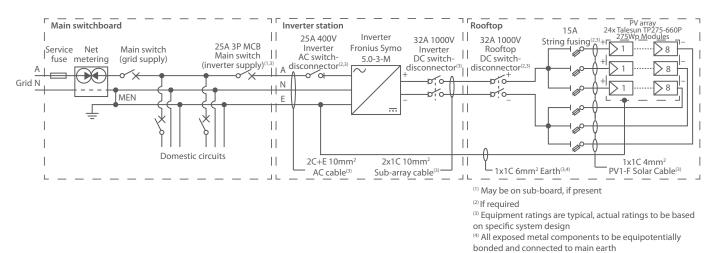


Figure 16.6a: An example of a electrical schematic of a grid-connected PV array.

Replacement of Figure 16.6b:

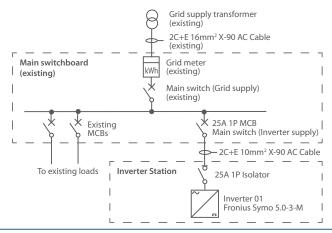


Figure 16.6b: An example of a SLD of a grid-connected PV array.

Chapter 19

19. Section 19.7 - Levelised Cost of Electricity (\$/kWh)

Amendment to Table 19.4:

| Year | Generation with 1% drop (kWh) | Present day value (kWh) |
|------------------------------------|-------------------------------|-------------------------|
| 1 | 20,000 | 19,626 |
| 2 | 19,800 | 19,067 |
| 3 | 19,602 | 18,523 |
| 4 | 19,406 | 17,995 |
| 5 | 19,212 | 17,482 |
| 6 | 19,020 | 16,984 |
| 7 | 18,830 | 16,500 |
| 8 | 18,641 | 16,029 |
| 9 | 18,455 | 15,573 |
| 10 | 18,270 | 15,128 |
| 11 | 18,088 | 14,698 |
| 12 | 17,907 | 14,279 |
| 13 | 17,728 | 13,872 |
| 14 | 17,550 | 13,476 |
| 15 | 17,375 | 13,092 |
| 16 | 17,201 | 12,719 |
| 17 | 17,029 | 12,356 |
| 18 | 16,859 | 12,004 |
| 19 | 16,690 | 11,662 |
| 20 | 16,523 | 11,329 |
| Life cycle energy generation (kWh) | | 302,394 |

Appendix

20. Appendices - Appendix 4

Addition to Glossary:

Passivated Emitter and Rear Cell (PERC): A high efficiency solar cell architecture that introduces a very thin passivation layer between the base silicon wafer and the metal contact on the rear surface.

21. Appendices - Appendix 5

Amendment to Chapter 14 Quiz Question 1b:

2% (Note the CEC Guidelines recommend a maximum of 1% rise between inverter and main switchboard, and local restrictions may apply.)